【書類名】　図面

【図1】

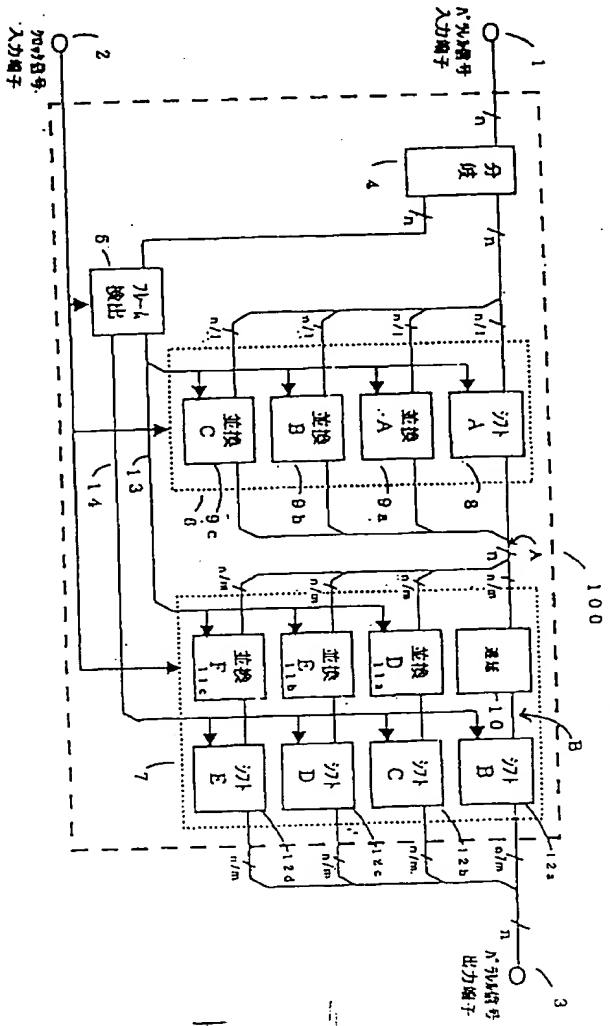

Fig. 1

[Fig. 1]

1: Parallel Signal Input Terminal

2: Clock Signal Input Terminal

3: Parallel Signal Output Terminal

4: Branch

5: Frame Detection

8: Shift A

9a: Sort A

9b: Sort B

9c: Sort C

10: Delay

11a: Sort D

11b: Sort E

11c: Sort F

12a: Shift B

12b: Shift C

12c: Shift D

12d: Shift E

【図2】

Fig 2

A1

シフト回路A～Eの真理値表(並び替え回路、シフト回路の入力が4ビットの時)

入力						出力			
D0	D1	D2	D3	SEL	CLK	Q0	Q1	Q2	Q3
A	B	C	D	0	↑	A	B	C	D
A	B	C	D	1	↑	B	C	D	A(+1)
A	B	C	D	2	↑	C	D	A(+1)	B(+1)
A	B	C	D	3	↑	D	A(+1)	B(+1)	C(+1)

A2　　A3

[Fig. 2]

Proof - 1999/11/29

A1: Truth Table of Shift Circuits A to E (Where Input of Sort Circuit and Shift Circuit is 4 Bits)

A2: Input

A3: Output

~~【図3】~~ Fig. 3

A1

並び換え回路A～Cの真理値表(並び換え回路の入力が4ビットの時)

入力						出力			
D0	D1	D2	D3	SEL	CLK	Q0	Q1	Q2	Q3
A	B	C	D	0	↑	A	B	C	D
A	B	C	D	1	↑	B	C	D	A
A	B	C	D	2	↑	C	D	A	B
A	B	C	D	3	↑	D	A	B	C

A2 A3

~~【図4】~~ Fig. 4

A1

並び換え回路D～Fのイネーブル時の真理値表(1ビットシフト回路の入力が4ビットの時)

入力					出力			
D0	D1	D2	D3	CLK	Q0	Q1	Q2	Q3
A	B	C	D	↑	B	C	D	A

A2 A3

~~【図5】~~

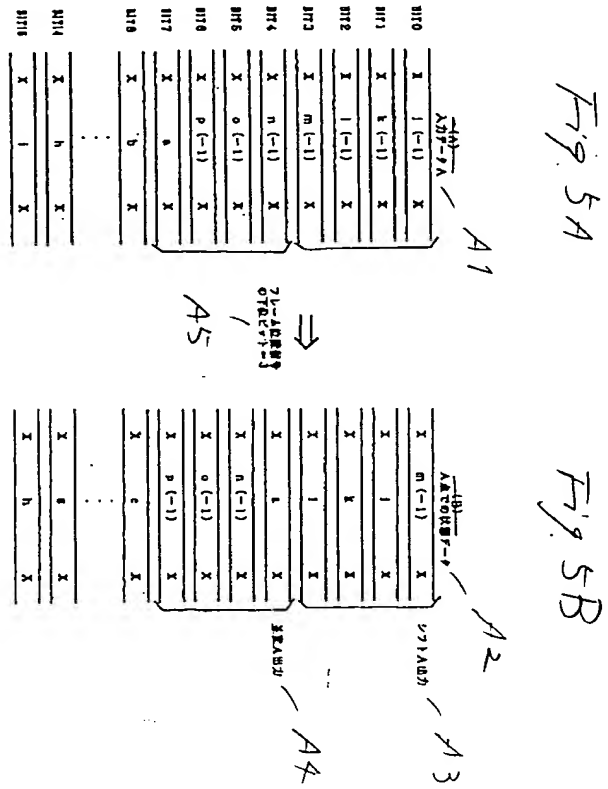

Fig. 5A

Fig. 5B

[Fig. 5A]

A1: Data Input A

[Fig. 5B]

A2: State Data at Point A

A3: Shift A Output

A4: Sort A Output

A5: Low Order Bit of Frame Position Signal

[Fig. 3]

A1: Truth Table of Sort Circuits A to C (Where Input of Sort Circuit is 4 Bits)

A2: Input

A3: Output

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[Fig. 4]

A1: Truth Table of Sort Circuits D to F in Enable (Where Input of 1 Bit Shift Circuit is 4 Bits)

A2: Input

A3: Output

~~【図6】~~

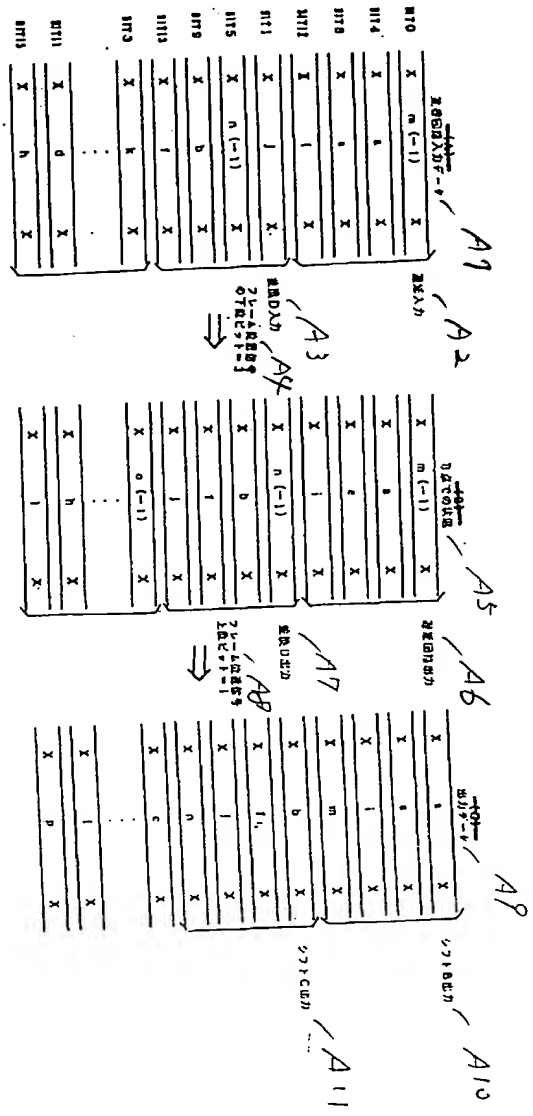

Fig 6A

Fig 6B

Fig 6C

[Fig. 6A]

A1: Input Data of Sort Circuit

A2: Delay Input

A3: Sort D Input

A4: Low Order Bit of Frame Position Signal

[Fig. 6B]

A5: State at Point B

A6: Delay Circuit Output

A7: Sort D Output

A8: High Order Bit of Frame Position Signal

[Fig. 6C]

A9: Output Data

A10: Shift B Output

A11: Shift C Output

【図7】

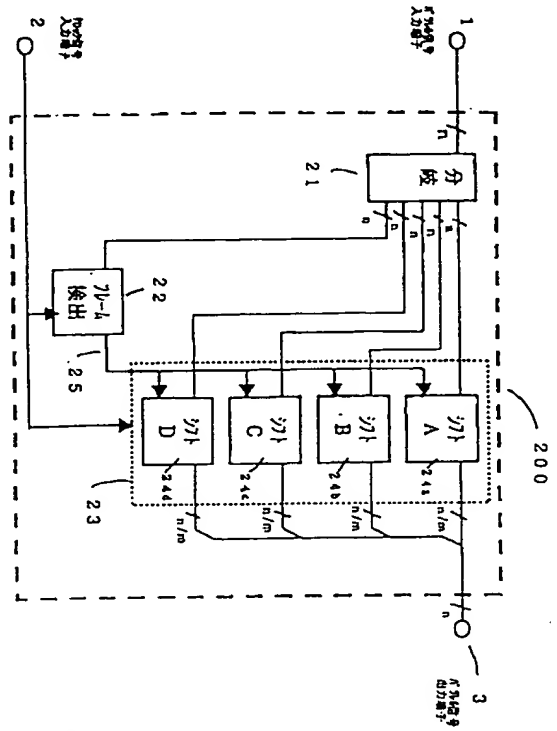

Fig 7

【図8】

Fig 8

シフト回路Aの真理値表(ﾃﾞｰﾀ入力が16ﾋﾞｯﾄ、シフト回路数が4個構成の時)

入力							出力			
D0	D1	D2	…	D15	SEL	CLK	Q0	Q1	Q2	Q3
A	B	C	…	P	0	↑	A	B	C	D
A	B	C	…	P	1	↑	B	C	D	E
A	B	C	…	P	2	↑	C	D	E	F
A	B	C	…	P	…	↑	…	…	…	…
A	B	C	…	P	15	↑	P	A(+1)	B(+1)	C(+1)

【図9】

Fig 9

シフト回路Bの真理値表(ﾃﾞｰﾀ入力が16ﾋﾞｯﾄ、シフト回路数が4個構成の時)

入力							出力			
D0	D1	D2	…	D15	SEL	CLK	Q0	Q1	Q2	Q3
A	B	C	…	P	0	↑	E	F	G	H
A	B	C	…	P	1	↑	F	G	H	I
A	B	C	…	P	2	↑	G	H	I	J
A	B	C	…	P	…	↑	…	…	…	…
A	B	C	…	P	15	↑	D(+1)	E(+1)	F(+1)	G(+1)

[Fig. 8]

A1: Truth Table of Shift Circuit A (Where Data Input is 16 Bits, and There are Four Shift Circuits)

A2: Input

A3: Output

[Fig. 9]

A1: Truth Table of Shift Circuit B (Where Data Input is 16 Bits, and There are Four Shift Circuits)

A2: Input

A3: Output

[Fig. 7]

1: Parallel Signal Input Terminal

2: Clock Signal Input Terminal

21: Branch

22: Frame Detection

24a: Shift A

24b: Shift B

24c: Shift C

24d: Shift D

3: Parallel Signal Output Terminal

【図１０】

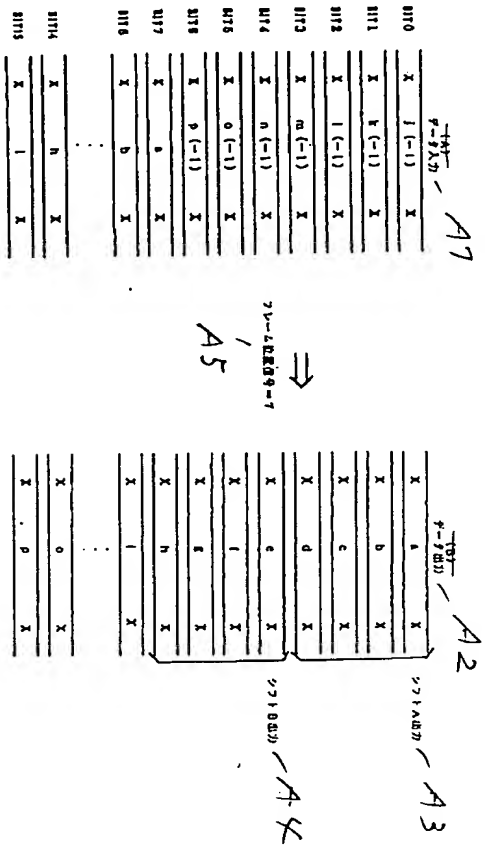

Fig. 10A

Fig. 10B

[Fig. 10A]

A1: Data Input

[Fig. 10B]

A2: Data Output

A3: Shift A Output

A4: Shift B Output

A5: Frame Position Signal

【図１１】

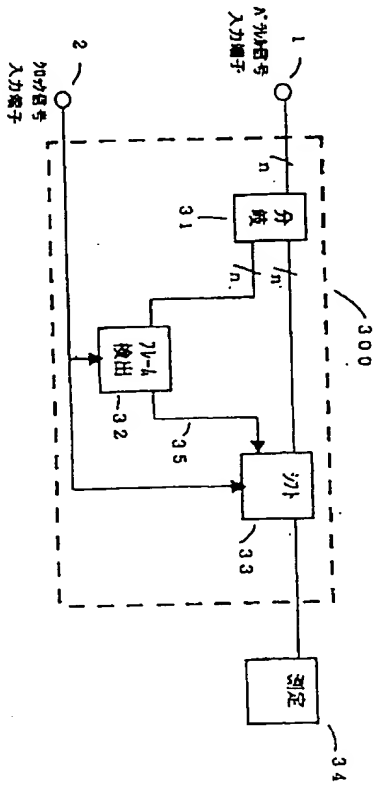

Fig. 11

【図１２】 Fig. 12

A1

シフト回路の真理値表(データ入力が16ビットの時)

入力							出力				
D0	D1	D2	…	D15	SEL	CLK	Q0	Q1	Q2	…	Q3
A	B	C	…	P	0	↑	A	B	C	…	P
A	B	C	…	P	1	↑	B	C	D	…	A(+1)
A	B	C	…	P	2	↑	C	D	E	…	B(+1)
A	B	C	…	P	…	↑	…	…	…	…	…
A	B	C	…	P	15	↑	P	A(+1)	B(+1)	…	O(-1)
A	B	C	…	P							

A2 A3

[Fig. 11]

1: Parallel Signal Input Terminal

2: Clock Signal Input Terminal

31: Branch

32: Frame Detection

33: Shift

34: Measurement

Proof - 1999/11/29

[Fig. 12]

A1: Truth Table of Shift Circuit (Where Data Input is 16 Bits)

A2: Input

A3: Output